Measurement and Analysis of Electrical Data for Silicon Nanowire Using Semiconductor Parameter Analyser

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Abstract—Nanowire based devices are becoming more promising, because size scaling in CMOS technology continues to follow Moore’s Law and hence device scaling based on the planar structures becomes difficult and is about to reach the end of the technology road map. Another factor is that, as the gate length shortens, the gate control over the channel degrades due to short channel effect and therefore, nanowire based devices were developed as an alternative to ultra-scaled CMOS devices. In this paper the results of measured and analysed electrical data for silicon nanowire will be presented. Two and four probe techniques of measuring electrical data for silicon nanowire were adopted while performing measurements. The paper will also present a review on the synthesis processes of silicon nanowire.

Keywords—Semiconductor parameter analyser, CMOS technology, Moore’s Law, probing techniques, silicon nanowire.

I. INTRODUCTION

Silicon nanowire is currently the promising nanostructure used as building block in microelectronics and optoelectronics devices like transistors, biosensors, memory elements, and interconnects, by definition a semiconductor (InP, Si, GaN, etc) nanowire is a structure with the diameter of the order of nanometre (10^{-9} m). Typical nanowires are often referred to as one-dimensional (1-D) materials with many interesting properties that are not seen in bulk (3-D) materials which is due to the quantum confinement of electrons laterally in silicon nanowire resulting in occupy energy levels that are different from the normal continuum of energy levels or bands found in bulk materials [1]-[2].

In order to make very good uses of silicon nanowire it is important to characterise a vast number of them with different cross-sectional shapes, sizes and axis orientation for their electronic properties. The results that will be presented here are the electrical measurements of highly n-type (phosphorus) doped samples of silicon nanowires with 8.5 X 10^{18} cm^{-3}, doping concentration.

Semiconductor nanowires are termed as special because of their technological and physical significance, the diameter puts the radial dimensions of these structures at or below characteristic length scale of many interesting and fundamental solid state phenomenon like the exciton bohr radius, wavelength of light, phonon mean free path, critical size of magnetic domains, exciton diffusion length and many others [3]. This radial dimension issues result alteration in many physical properties of the semiconductors within the confinement of the nanowire surface and also their large-surface-to-volume ratio allows for distinct structural and chemical behaviour as well as greater chemical reactivity [4]. Silicon nanowires are ideal for sensor applications where large surface-to-volume ratio can be exploited.

II. BACKGROUND

The venture into the field of nanowire devices was first published in 1964 where detailed studies of the morphology and growth of silicon whiskers (smaller than ordinary human hair) from the vapour was reported [5]. In 1975 the oriented growth of GaAs, GaP, InAs and GaInAs whiskers was also reported.

Figure 1 shows a histogram showing the intensive venture into the researches related to silicon nanowire and whiskers from 1963 to 2007 [6]-[7]. Latter in 2012 a report on fabrication of silicon nanowire on “SILICON-ON-INSULATOR” substrate using top-down approach comprising film deposition, photolithography and etching was reported [8].

III. SYNTHESIS OF SILICON NANOWIRE

The unique properties of silicon nanowire arising from small dimensions as introduced earlier is the key factor that make them the driving force in the field of microelectronics and memory device applications. There are various types of methods that can be used to fabricate silicon nanowires which are categorised as bottom-up and top-down approaches. Number of publications mentioned that the latter has been used predominantly to fabricate small patterns down to a few nanometres in size as well can enable the best control over the
feature size and placement for creating patterns on wafers with large diameter at low cost and high throughput because of the following distinctive features of silicon nanowires fabricated by bottom-up approach.

1. Very small diameter nanowires are possible with this method.
2. Possibility of in-situ doping.
3. Heterogeneous composition.
4. Fewer surface dangling bonds.

IV. Top-Down Approach

This method of fabricating silicon nanowire is termed as subtractive approach in which curved structures can be formed from a larger piece of material via film deposition, photolithography and etching as was the case in the fabrication process of CMOS devices [8].

Fig. 2 shows the experimental procedure to fabricate silicon nanowire using this approach:-

Fig. 2 Fabrication of silicon nanowire using top-down approach [8].

(a) First KOH etching.
(b) Thermal oxidation of resulting Si (111) plane.
(c) Wet etching using phosphoric acid.
(d) Second KOH etching to expose other diagonal of Si (111).
(e) Triangular nanowire.
(f) Further etching to remove BOX to leave a free standing nanowire.

V. Bottom-Up Approach

This method is based on two observations.

1. Addition of certain metal impurities is an associated pre-requisite for growth of silicon nanowires in the experiment.
2. Small globules of the impurity (gold or silver) are located at the tip of the wire during growth.

Based on the above observations figure 3 shows the strand vertically grown silicon nanowire as where the globule at the wire tip act as the preferred sink for the arriving silicon atoms or as catalyst for the chemical process that are associated with this growth technique [9].

VI. Methodology

In order to control the electrical properties of silicon nanowires, it is important to characterise their electronic transport properties. Semiconductor parameter analyser (Agilent 4155C) was used to prove nanowire structures on silicon wafer and characterised the electronic transport in these structures. This was done by applying a biasing voltage sweep and recording the I-V data results which was analysed and obtained some parameters such as contact resistance, nanowires resistance, and resistivity of nanowires and then analysis of the change of resistance with dimensions such as length, and area were determined.

The dimensions of the triangular silicon nanowire with nanometric height and µm length in figure 4 can be obtained using atomic force microscopy (AFM).

Fig. 3 Schematic of silicon nanowire growth by bottom-up approach [10].

(a) Gold or Silver when deposited on a silicon substrate and then heated to a temperature of about 400°C forming a small liquid Au-Si alloy droplet.
(b) Exposing such a substrate to a precursor gas (SiCl₄ or SiH₄), the precursor’s molecules will crack on the surface of the Au-Si alloy droplet and the silicon will be incorporated into the droplet and the silicon from the gas phase causes the droplet to become supersaturated with silicon until the silicon freezes out at the interface.
(c) When the above process is continually repeated, the resulting strand of a silicon nanowire with the alloy droplet riding atop is realised.

The diameter of the nanowire is determined by the size of the Ag or silver droplet [10].

Fig. 4 AFM image revealing the surface structure and dimensions of a silicon nanowire
(a). Probe Station and Agilent 4155C Semiconductor Parameter Analyser

The electrical characterisation (I- V measurements) of silicon nanowire presented in this paper was performed at probe station by placing the wafer on the chuck. The wafer was held in position with help of vacuum so that the sample is free of movement to enable selection of device piece on the wafer surface as well as proper probe- to-sample electrical contact using the microscope. Adjacent (side by side) movement of chuck is also possible to enable proper alignment and accurate device positioning. The cables were attached to back of the probe station. To avoid sample destruction sure was made that the lever is upright and then gently drawn downward for smooth probe- to-sample contact.

The probe station is connected to a typical bench top device used in advance device characterisation called ‘Semiconductor Parameter Analyser’. Desktop easyEXPERT software was used to operate the device even though it can be manually operated.

(b). Measurements of Electrical Data for Silicon Nanowire

When the physical conditions like temperature, dimension and mechanical stress of silicon nanowire remain unchanged then the potential difference between two points of the wire is proportional to the current flowing through it, where the constant of proportionality is called the resistance of the wire that depends on the length and the cross-sectional area as given by equation (4a). Generally the constant of proportionality is called the resistivity of the silicon nanowire material measured in Ωm.

(i). Two probe measurements

For a long thin silicon nanowire with uniform cross-section like the one (conduction channel in mosfet) shown in fig. 5(a) the resistivity can be measured by measuring the voltage drop across the nanowire due to passage of current through the wire. The nanowire with cross-sectional area, and length, has resistivity given by equation (4a).

The source supply a current measured in ampere by the ammeter connected in series with the supply and the voltage (potential difference) between the two contacts at the end of the silicon nanowire is measured by the voltmeter that is connected in parallel to the source.

(ii). Four probe measurements

In four point probe measurements the tips controlled by mechanical screws that travel up and down are equally spaced during probing for electrical data extraction. In this method of measurement sure was made that the surface on which the probes rest is flat so that surface leakage apart from contact resistance is eliminated as well.

In figure 6, the current supplied through two outer probes (A and B) is from the high impedance source while the voltmeter is used to measure the voltage across the two inner
probes (X and Y) and with this it easy to determine the resistivity of the nanowire on bulk silicon. Moreover this high input impedance voltmeter prevents the two inner probes from drawing current and hence unwanted voltage drop at point X and Y caused by contact resistance between probes and nanowire is isolated from measurements [11]-[12].

VII. RESULTS AND DISCUSSIONS

The electrical data for the highly doped silicon nanowire like the conduction channel in MOSFET was measured using two and four probe I-V measurements methods and in order to measure the electrical conductivity of the silicon nanowire voltage sweep between 0v to 10v was applied while recording the corresponding current values. The disadvantage of the two-probe contact approach is that the contact resistance leads to measurement error and it cannot be used for non-planar structures with random shapes. Electrical data of silicon nanowire can be obtained with help of ohm’s law presented in the below equations;

\[ J = \sigma E \]  \hspace{1cm} (1)

\[ J = evn \]  \hspace{1cm} (2)

\[ V = IR \]  \hspace{1cm} (3)

Where, \( R \) is the resistance and \( V \) is the voltage. In other way it can be written as:

\[ R = \frac{\rho L}{A} \]  \hspace{1cm} (4a)

\[ \rho = \frac{VA}{IL} \]  \hspace{1cm} (4b)

Where resistivity (\( \rho \)) is the reciprocal of conductivity.

The result of the Current – Voltage characteristic measurements for highly n-type doped silicon nanowire having 17\( \mu \)m length and 48nm thick with initial bulk silicon (n-type) doping concentration of 8.5 \( \times \) 10\(^{18} \) cm\(^{-3} \) is presented in the I-V curve in figure 7. This is done to prove the electrical continuity of and to see that an electrical contact has been established between the deposited metal and the silicon nanowire. For the triangular silicon nanowire grown over 54\(^\circ \) crystal orientation with thickness of 48nm equivalent to a cross-sectional area of approximately 1700nm\(^2 \), the resistance was found to be approximately 400M\( \Omega \) corresponding to a nanowire resistivity of 0.039\( \Omega \)m. The dimensions of this particular nanowire allowed the chance of using it for sensor applications.

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REFERENCES


